



Technology Analysis of Nanotechnology for ICT Manufacturing Technologies

Table of Contents

Table of Contents	2
1. Manufacturing Technology	3
1.1. Definition	3
1.2. Definition	3
1.2.1. Immersion Lithography	3
1.2.2. Extreme Ultraviolet Lithography	4
1.2.3. Computational Methods	4
1.3. State of R&D	5
1.3.1. Nanoimprint Lithography	5
1.3.2. Electron Beam Write Direct Lithography	6
1.3.3. Scanning Beam Interference Lithography	6
1.3.4. Dip Pen Nanolithography	6
1.3.5. Reactive Ion Etching	7
1.3.6. Scanning Probe Lithography	7
1.4. Additional demand for research	8
1.5. Applications and perspectives	9
1.6. Key players and experts (selection)	10
1.6.1. Projects, Industry Associations, etc.	10
1.7. References and Literature (selection)	11

1. Manufacturing Technology

1.1. Definition

Manufacturing technology for electronics is a field of intense activity. Moore's Law, which states that every 18 months, the transistor density of semiconductor chips should double, provides an impetus to continually miniaturise integrated circuit components.

This report looks at manufacturing technologies which can be applied to nanoelectronics applications. These include continued developments of lithography, as well as novel methods such as nano-imprint lithography.

1.2. Definition

The current approach to producing transistor chips employs photolithography. The basic process involves applying a photoresist material to a substrate wafer (possibly by spin coating). Light is then applied to the wafer through a mask, which renders soluble the photoresist material upon which the light falls. A developer solution is then used to remove the soluble photoresist. The material that is not protected by the remaining photoresist is etched away. Finally the photoresist material is also removed. The light source used is currently deep ultraviolet.

A limit which now comes into play is that lithography techniques are limited in how small they can scale by the wavelength of the light source used. This has been addressed with several approaches which scale existing technology and which, whilst perhaps not being classical nanotechnology, are still worth describing here.

These approaches obtain smaller feature sizes by adjusting three parameters of the manufacturing process; scaling the wavelength of the light source uses (as in EUVL), increasing the refractive index of the immersion medium, or increasing the k_1 factor (a term which covers several of the error sources in the lithography process).

1.2.1. Immersion Lithography

Immersion Lithography employs a liquid between lens and wafer which has a refractive index greater than one. This enables scaling down the wavelength of the light source. The immersion medium that is typically used is highly purified water, which creates feature sizes of 37nm. Immersion lithography is seeing industrial adoption.

1.2.2. Extreme Ultraviolet Lithography

Extreme Ultraviolet Lithography (EUVL) uses mirrors to focus the UV beam, enabling the creation of sub- 100nm feature sizes. The EUVL wavelength is 13.5nm. The process occurs in a vacuum, so that air molecules do not distort the EUVL beam, and requires highly reflective optics so that the beam is not distorted nor stripped of power.

One of the new features of the EUVL is the increased energy of the EUVL photons, which leads to roughness of the feature sizes. Groups at CNSE in New York and at IMEC in Belgium are developing test chips with EUVL, reporting feature sizes of 60-90nm.

Challenges in the development process of EUVL, has set back the introduction of this technology. The most pressing obstacle is the identification of reliable high power sources, followed by the challenge of producing defect free masks. Identifying suitable resist materials, which was a major obstacle, has shown progress recently. The suggestion is that EUVL will not be introduced until 2012 at the earliest, at the 16nm node.

1.2.3. Computational Methods

The third approach to scaling existing lithography processes is to use computational methods to optimise? adapt 193nm wavelength light sources to create 32nm and even 22nm feature sizes.

Process elements that can be optimised include the layout of the masks and the intensity of illumination at different points. One example is to reduce the intensity of the light source at points where multiple detailed features are close together, to avoid roughness in the patterning of the substrate.

This type of process modelling has highly intensive computing requirements, given the number of factors that must be analysed.

1.3. State of R&D

The chapter address nanotechnology-based manufacturing technologies with a primary application to create integrated circuits or other electronic devices. More general manufacturing methods, such as Molecular Beam Epitaxy (MBE), and Chemical Vapour Deposition (CVD) are covered in other ObservatoryNano reports.

1.3.1. Nanoimprint Lithography

This technology was first described by Stephen Chou et al. in 1995. Nanoimprint Lithography is conceptually a rather simple technology, relying on mechanical deformation of the media which is patterned.

A number of techniques can be used to pattern features onto a stamp. This may include electron beam lithography; because one stamp is created which can then be used multiple times, the low speed of e-beam lithography is outweighed by it's accuracy.

The stamp is then applied to a substrate. This may involve heating the substrate (thermal nanoimprint) so that the surface deforms when the stamp is applied. Another technique, UV nanoimprint, applies both UV-light and pressure to the stamp and substrate. This technique appears to meet high-volume throughput requirements. It is also possible to directly pattern some materials, including aluminium and silicon.

The printing of the stamp onto the substrate creates a contrast thickness pattern. The part of the pattern which is compressed can then be removed using normal etching process.

Nanoimprint technology has a number of advantages. It is relatively inexpensive when compared to deep UV methods, which has meant that it is particularly suitable for experimental and low volume production. The technique has also been applied to create nanoscale devices other than electronic circuitry, such as sensors and micro-fluidic devices.

Nanoimprint lithography is an active field with a number of companies and research groups working in this space. However, nanoimprint is not yet considered to be a viable candidate to supplant UV lithography in semiconductor fabrication, due to concerns over the scalability of the technology – a combination of the time required to pattern stamps, the area that can be patterned by the stamps, and the durability of the stamp itself, given the mechanical nature of the manufacturing process.

1.3.2. Electron Beam Write Direct Lithography

Electron Beam Write Direct Lithography involves scanning an electron beam across a surface, exposing areas of this resist. This is a maskless technique, as the electron beams are directly applied to the surface. Industrial scale equipment for e-beam lithography is very costly, but it is possible to adapt a Scanning Electron Microscope (SEM) for e-beam lithography – this has made it possible for more research groups to use the technology.

The advantage of e-beam lithography is that the beam itself can be directed very precisely, leading to the creation of very exact feature sizes. This means that limitations of the resolution of this technique are caused not by the beam itself, but by its behaviour when it interacts with the photoresist. Electron scattering can reduce the pitch of feature sizes that is achievable, though this in turn can be reduced by using lower energy electron beams.

The serious limitation of e-beam lithography is that it is very slow, given that it is essentially drawing every feature onto a wafer. Throughput when patterning a whole 300mm wafer (the largest size currently in production) would be measured in years rather than minutes.

1.3.3. Scanning Beam Interference Lithography

An optical lithography technique, scanning beam interference lithography employs two lasers which interfere with each other.

In practice it is necessary to move the wafer under the scanning beam in order to pattern larger areas. This in turn creates a problem of Doppler shifts caused by the movement of the wafer relative to the lasers. A scanning beam process developed by Mark Schattenburg at MIT uses sound waves to accurately gauge the position of the wafer and to adjust the scanning beam accordingly.

1.3.4. Dip Pen Nanolithography

Dip Pen Nanolithography (DPN) was developed by Chad Mirkin at Northwestern University. The technique uses the tip of an atomic force microscope (AFM) to transfer a substance to a surface. The process is analogous to a pen being dipped in ink and then drawn across paper.

In order for the ‘ink’ to transfer from the AFM tip to the substance to be patterned, the whole process occurs in humid atmosphere. This causes moisture to gather on the end of the AFM tip, which in turn transfers the ‘ink’ to the substrate with a capillary action, leaving the tip itself clean.

This technique has been used to generate patterns with line widths of as little as 10-15nm. Despite its low speed, the precision of the technique has made it suitable for low volume and experimental use. Indeed, flexibility in the choice of 'ink' has also led to the use of DPN in biological applications.

1.3.5. Reactive Ion Etching

Reactive Ion Etching (RIE) can take place as a component of normal photolithography processes. It is an etching technique, which is used to remove excess material after a patterning process. The process itself involves using an electromagnetic field to create a plasma, which delivers ions vertically, showering the surface of a wafer. Positive ions interact with the surface features, transferring kinetic energy which removes some of the material. The vertical delivery of ions leads to very sharp vertical (anisotropic) etching of features.

1.3.6. Scanning Probe Lithography

Scanning probe lithography really describes a number of techniques which employ an STM or AFM tips to pattern a substrate (though this is a distinct field from DPN). These include directly patterning the substrate by scratching, indenting or local heating. The Quate group at Stanford is developing methods which use an STM to generate an intense, local electrical field. This could be used in field enhanced oxidation, in which the electrical field causes a material, such as silicon, to oxidise. With the same starting point, the SPM tip can be used as a field emitter, applying a stream of electrons to a thin resist, causing changes in the resist material.

1.4. Additional demand for research

Demand for research can be analysed on two levels. Firstly, there are improvements to these nanotechnology based techniques which would increase their applicability to a wider range of higher volume applications. A more challenging development goal is for these technologies to be able to compete with extensions to existing lithography-based methods for the production of integrated circuits – one of the most heavily optimised, costly and demanding manufacturing processes in existence.

Nanoimprint technology, which is a generally promising approach with a number of applications, still faces some development challenges. These require more study of the actual stamping process, including how to pattern over larger areas whilst managing pattern overlap and avoiding misalignment of stamps.

Throughput is a key factor in enabling or preventing the adoption of these technologies in semiconductor fabrication. A production fab is currently able to process up to 100 wafers per hour using optical lithographic techniques. EUVL, thought to be one of the successor methods, is only able to produce around 2.5 wafers per hour.

1.5. Applications and perspectives

The ultimate application of these manufacturing technologies is semiconductor fabrication. However, before that point there are a number of applications for which nanoimprint lithography and other techniques may be better suited in the short to medium term. These include:

- High Brightness LEDs
- Storage media
- MEMs
- Flat Panel Displays
- Flexible Electronics

Both NIL and DPN may also have applications in biomedical fields, producing devices such as biosensors.

1.6. Key players and experts (selection)

1.6.1. Projects, Industry Associations, etc.

Emerging Nanopatterning Methods (NaPa),

<http://www.phantomsnet.net/NAPA/index.php?project=3>

Nanopatterning, Production and Applications based on Nanoimprint Lithography (NaPANIL),

<http://www.napanil.org/>

(A FP7 project with 18 partners, lasting from May 2008 to April 2012).

Maskless Lithography for IC manufacturing (<http://magic-fp7.org/>)

(FP7 Project, includes Mapper Lithography, IMS Nanofabrication AG of Austria,

STMicroelectronics, CEA-Leti, Synopsys, Qimonda, KLA-Tencor, Fraunhofer and others.)

1.7. References and Literature (selection)

- Intel: 'EUV Facts Don't Add Up' for 22 nm in 2011 (2008), Semiconductor International,
<http://www.semiconductor.net/article/CA6553758.html>
- IBM rolls 'computational scaling' for litho at 22-nm (2008), EE Times,
<http://www.eetimes.com/showArticle.jhtml?articleID=210602297>
- Second impression for nanoimprint (2007) EE Times,
<http://www.eetimes.com/showArticle.jhtml;jsessionid=ENZ2BULAASNUQSNDLRSKH0CJUNN2JVN?articleID=199902420>
- 10 fab technologies on the hot seat (2008) EE Times,
<http://www.eetimes.com/showArticle.jhtml;jsessionid=ENZ2BULAASNUQSNDLRSKH0CJUNN2JVN?articleID=210604050>
- EUV most likely litho for 22-nm node, says IMEC's Ronse (2008), EE Times,
<http://www.eetimes.com/showArticle.jhtml;jsessionid=ENZ2BULAASNUQSNDLRSKH0CJUNN2JVN?articleID=211202013>
- Intel Silicon & Manufacturing Update (2007), Intel,
http://download.intel.com/pressroom/kits/events/idffall_2007/BriefingSilicon&TechManufacturing.pdf
- Nano World: Roadmap for nano-imprinting (2006), Physorg,
<http://www.physorg.com/news65451782.html>
- Chou et al (1996), J. Vac. Sci. Technol. B 14(6), Nov/Dec 1996, Nanoimprint lithography,
Available at <http://www.nanonex.com/nanoimprint.pdf>
- Mirkin Group, Northwestern University [Accessed 22 Jan 2009],
<http://chemgroups.northwestern.edu/mirkingroup/dpn.htm>
- Carlberg (2006), Development of Nano-Imprint Lithography for Applications in Electronics, Photonics and Life Sciences. Lund University Doctoral Thesis,
<http://www.patrickcarlberg.dk/Download%20area/Dissertation%20no%20articles.pdf>
- Introduction to Scanning Probe Lithography, Quate Group, Stanford University,
http://www.stanford.edu/group/quate_group/Litho/LithoPages/Introduction/Introduction2.html
- Nanoimprint lithography presses into manufacturing markets (2007), Small Times,
http://www.smalltimes.com/articles/article_display.cfm?Section=ARCHI&C=Elect&ARTICLE_ID=286744&p=109

Balla et al (2008), J. Phys. D: Appl. Phys. 41, An assessment of the process capabilities of nanoimprint lithography