



Technology Sector Report

**Technology Analysis of Nanotechnology for
Integrated Circuits**

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1. Definition

This ICT sector sub-report examines nanotechnology-based developments in complementary metal oxide semiconductor (CMOS) integrated circuits. In this report, the focus is on short to medium-term developments based or derived from silicon technology. Long-term developments are considered in sub-report “Beyond CMOS”. Manufacturing issues are discussed in sub-report “Production technologies”. Development of memory technologies is described in sub-report “Memory”.

2. Short description

As the number of functions that can be integrated on a single chip or package grows exponentially, so grow the associated technological challenges. In the semiconductor industry, R&D has been structured into parallel technology domains, in order to be able to draw clear roadmaps and assign research priorities. This report is structured according to this following division.

The domains are:

1. **“More Moore” (MM):** minituarisation / scaling
The MM domain is defined as an attempt to further develop advanced CMOS technologies with the objective to continue “Moore’s Law” (the prediction that the cost-per-transistor on a silicon chip will halve every two to three years). This technology domain continues to target reduction of device dimensions in order to improve density (cost per function reduction), performance (speed, power) and reliability values. It also includes the development of new processes and materials that improve device performance.
2. **“More than Moore” (MtM):** diversification
The MtM domain refers to a set of technologies that enable non-digital functions (e.g., RF communication, power control, passive components, sensors, actuators). They do not necessarily scale according to “Moore's Law,” but provide additional value to the end customer in different ways. From the application perspective, MtM allows interaction with people and the environment. This includes conversion of non-digital and non-electronic information (such as mechanical, thermal, acoustic, chemical, optical and biomedical functions) to digital data and visa versa, providing a functional diversification to the CMOS based digital information processing.
3. **“Heterogenous integration” (HI) :** higher value systems
The HI domain refers to “System-in-Package” (SiP) solutions in which a combination of MM and MtM components are integrated together. These are multifunctional systems in which digital and non-digital functionalities are integrated into compact packages with IC dimensions.
4. **“Beyond CMOS”:** disruptive technologies
The Beyond CMOS domain refers to a set of disruptive functions that, in the long term, will complement or replace conventional silicon technology. These technologies are described in the ICT sector sub-report “Beyond CMOS”.

The semiconductor industry carries out extensive road mapping exercises in order to agree on key research priorities for these domains. Internationally, the main agreed foresight of research is consolidated in the International Technology Roadmap for Semiconductors (ITRS). The objective of the ITRS is to ensure cost-effective advancements in the performance of the integrated circuit and the products that employ such devices, thereby continuing the health and success of this industry.

At European level, the European Nanoelectronics Initiative Advisory Council (ENIAC) has set up a “strategic research agenda” (SRA) that emphasizes the areas of particular interest for European-based research.

This report summarises the main research priorities reported in the ENIAC Strategic Research Agenda (SRA) and ITRS 2007 Edition from nanotechnology enabled development perspective.

2.1. “More Moore” domain

Almost 70% of the total semiconductor components market is directly impacted by advanced CMOS miniaturization achieved in the More Moore domain. This 70% comprises three component groups of similar size: microprocessors, mass memories, and digital logic.

During the last decades, the smallest pattern sizes on silicon wafers have been reduced from 6 - 8 microns to around 20 nanometres. Similarly, manufacturing relied on 25-mm diameter wafers, whereas today it's done on 300 mm wafers. New technology generations continue to be introduced every 2-3 years. At the same time, the number of technical challenges increases. In addition to geometrical scaling, material and architecture innovations will play a more important role in the future to enable further increases in device performance. By combining silicon innovations with other novel nanotechnologies, it is expected that Moore's Law will extend well into the next decade (until 2015).

Continuous size reduction of CMOS transistors (the basic building blocks of logic circuits) has produced enhanced performance for decades in terms of speed, power consumption, reliability and cost per function. Now significant challenges are expected. The conventional path of scaling, which was accomplished by reducing the gate dielectric thickness, reducing the gate length, and increasing the channel doping, might no longer meet the application requirements set by performance and power consumption. Introduction of new material systems as well as new device architecture, in addition to continuous process control improvement are needed to break the scaling barriers.

In the following, the main technologies and key research priorities for development of advanced CMOS transistors are described. Development of memories is discussed in ICT sector sub-report “Memories”.

2.1.1. High-k dielectrics

Reduction of the gate oxide thickness has emerged as the most difficult challenge associated with the future device scaling. Ultra-thin gate dielectric suffers from a significant tunnel leakage current. Consequently, it is necessary to replace the conventional gate insulator, SiO₂, with a “high-k” (high permittivity) material for low power consumption. It is also necessary to introduce new metals that are compatible with the high-k material to replace the polysilicon gate electrodes.

These new materials, along with the right manufacturing process, are expected to reduce gate leakage more than 100-fold, while improving the transistor performance. Reduced gate leakage will also enable the devices to run cooler.

Alternative “high-k” materials are being researched intensively. Hafnium compounds are the most promising alternatives that are now being adapted to commercial production starting at

the 45-nm technology generation (node). Intel's new 45nm technology is using hafnium-based circuitry.

New high-k material will also require a new manufacturing process to lay down a thickness of one molecular level at a time. The new materials are typically deposited using atomic layer deposition (ALD). This is a thin-film deposition technique that can potentially be used for high-k gate oxides, high-k memory capacitor dielectrics, ferroelectrics, and metals and nitrides for electrodes and interconnects. ALD is also used in Intel's 45 nm process.

2.1.2. Technology and device architectures for multi-gate and multi-channel devices

More sophisticated transistor architectures will be needed in the future. This is necessary because electrostatic control of the gate becomes more challenging and the variability of the transistor characteristics may alter the functionality of logic gates as feature sizes are scaled down. New three-dimensional device architectures, such as multiple-gate FETs (MuGFETs) or multiple-channel FETs (MuCFETs), are expected. The process complexity needed to fabricate these devices has so far prevented their early introduction into manufacturing. The 22-nm node will probably be the entry point for these technologies.

2.1.3. Innovative solutions for interconnects

The performance of the interconnects between transistors is expected to pose problems. The effective resistivity of copper interconnects increases at small dimensions and the dielectric constant of the insulating film below and between the interconnect layers does not scale much. As a result, signal integrity in the connections is becoming a major issue. Long-term innovations, such as self-assembled nanoporous dielectrics with enhanced structural strength, air-gap dielectrics and 3D interconnects, will require major development work. Carbon nanotubes and silicon nanowires are alternatives under study.

2.1.4. Developing physical understanding of the limits of transistors

In order to prepare for long-term solutions, it is necessary to develop a physical understanding of the limits of transistors, e.g. transport physical mechanisms, device matching, impact of atomic-level statistical fluctuations, reliability limitations, and finally prepare the co-integration of CMOS with novel "Beyond CMOS" structures.

The research community is looking for ways to integrate III-V semiconductor materials to the silicon substrate because of the potential performance and power benefits. This compound semiconductor solution could be applicable to communications and optoelectronic circuits, which could potentially be integrated with CMOS logic on the same silicon chip. In the future, III-V devices and silicon CMOS transistors may coexist on the same silicon chip for increased performance and functionality with enhanced energy efficiency.

2.2. "More-than-Moore" domain

The technologies in the More-than-Moore domain provide functionality beyond the traditional digital computing. In order to interface with the real world, intelligent systems need to have

power, RF interfaces, sensor and actuator functions. MtM technologies provide added value on top commodity CMOS product portfolios and they also drive the development of emerging markets. Much effort is needed to master the heterogenous integration of the digital and non-digital functions into the same system.

Nanotechnology is expected to provide a significant impact to the development of several key areas, such as

- sensors and actuators
- RF technologies
- power
- thermal management
- user interfaces

An extensive overview of these developments is not within the scope of this report, but some aspects are briefly introduced in the following. Many of these issues are discussed in more detail in other reports (e.g. ICT sector reports on “Displays” and “Photonics”).

2.2.1. CNT and nanowire applications on CMOS platforms

A handful of electronic products made with carbon nanotubes (CNT) are already commercially available. Examples are CNT sensors, probe tips and transparent conductive films. As one of the novel solid materials, nanowires have also received much attention from the R&D community as components for electrical circuits, sensors or light-emitting sources based on CMOS compatible processes. Although the R&D activities for CNT and nanowires were initiated to address the future need of IC technologies beyond the physical limits of CMOS, more and more R&D activity nowadays is devoted to using CNT and nanowires to create new functionalities on top of the CMOS platform.

2.2.2. Sensors and actuators

Sensors and actuators are used almost everywhere to sense and monitor parameters and to correspondingly control actions of importance and interest in our daily environment. In many cases the fabrication processes and materials used to produce the sensor or actuator are not compatible with CMOS platforms.

The integration aspects of sensors and actuators onto CMOS platforms will be an important challenge for the years to come. This will include the development of sensors and actuators based on materials other than silicon (for example, III/V or plastic materials) that offer new functionality or lower cost, as well as arrays of sensors and actuators of the same or different functionality. New sensor types such as nanowires and carbon nanotubes with potential for improved sensitivity need to be investigated and fabrication processes have to be developed to integrate such new sensing elements into devices, systems and applications.

More research effort is needed for nanoscale sensors. Silicon nanowires and carbon nanotubes (CNT) show considerable potential for use as strain and deflection sensors, with high gauge

factors being reported for experimental structures. The major challenge is large-scale, well-controlled fabrication and integration of these nanoscale structures into sensor devices.

Of high importance for MtM is interfacing the extremely small signals generated by these nanoscale devices to microscale electronics. New analog circuit interfaces will be needed to exploit the extremely small signals from nanoscale sensors and NEMS (nanoelectromechanical systems) operating as individual devices or dense arrays.

2.2.3. Biosensors

A wide range of sensor types will be required for biological and biomedical applications. Nanotechnology is becoming a powerful enabler for new innovations, such as biochemical sensors, sensors for liquid and gas spectroscopy, ion-sensitive devices and sensors for detecting parameters such as CO₂ levels, ozone concentrations, fuel and oil conditions, hydrocarbons and gas.

Biosensing and bioanalysis are experiencing a paradigm shift in which complete biological assays are integrated into a single device, such as a disposable cartridge with an embedded “lab on a chip”. Such cartridges will typically integrate many different devices and materials. Such heterogeneous integration requires developing techniques for chemical surface engineering, biocompatible packaging, microfluidics, electrochemistry, nanostructures and integrated optics. In particular, fluid handling at chip level will present a major challenge.

Key research priorities in this area include development of biocompatible materials and processes, increasing biosensor sensitivity and specificity and development of biosystem package solutions (including signal processing, energy control, data treatment and data transmission).

2.3. “Heterogeneous integration” domain

The future of electronics will be smart multifunctional systems linked into networks, containing both electrical and non-electrical functions and used in a variety of applications. Future integration technologies must be able to successfully combine different technologies while also meeting yield and cost requirements, and achieving failure rates a thousand times better than today.

The extreme levels of system miniaturisation facilitated by nanotechnology also means that in many cases different nanodevices based on different technologies and processes will need to coexist within the same package. This is a significant shift away from traditional systems where functionality is typically separated into different boxes or packages.

System-in-Package (SiP) solutions combine digital and non-digital components that are integrated into packages with IC dimensions. The key technology underlying SiP is heterogeneous integration. This not only allows the integration of multifunctional components into one package, but includes the interface between nanoelectronic devices and systems that humans can interact with.

3D integration is a promising solution to achieving a high degree of system miniaturisation and multifunctionality is 3D system integration. This is an emerging solution that minimizes interconnection lengths and eliminates speed-limiting intra-chip and inter-chip interconnects. It

also has the potential for low-cost fabrication. However, 3D technologies will need to be tailored to the needs of the application they will serve.

Nanotechnologies will be used to optimize material properties, create new interconnects and develop new assembly technologies. New potential technologies include e.g. printable interconnects, self-alignment and self-assembly. These, however, will have to demonstrate their ability to allow high productivity at reasonable costs.

In the mid-term (until 2013), the addition of nanoparticles will provide a means of adjusting parameters such as electrical resistance, thermal conductivity, coefficient of thermal expansion, and coefficient of expansion due to moisture (e.g. for polymer materials). Interconnects can be improved using nanostructures that allow surface activated bonding and provide nanopillar contact bumps.

In the long term, nanotechnologies will be used to develop new nanoscale interconnects and self-assembly technologies. Possible applications include carbon nanotubes (CNT) for heat dissipation and interconnects, low-temperature interconnects using nanostructured surfaces, self positioning or self-assembly of devices and molecular bonding. Key aspect in the development of these technologies is demonstrating their ability to allow high productivity at reasonable costs.

3. Additional demand for research

For decades, enhanced performance of integrated circuits has been achieved largely by shrinking transistors and wires to pack more power into smaller space. Now major problems are arising due to heat generation, an increasing number of defects and basic principles of physics.

Introduction of new material systems as well as new device architecture, in addition to continuous process control improvement are needed to break the scaling barriers. The industry is already looking beyond conventional silicon technology and moving to the world of nanoscale structures.

Additional research is needed to develop alternate strategies to extending the current CMOS platform such that performance and energy efficiency requirements are fulfilled. An important aspect is adding functionality and creating integrated circuits that can be adapted to specific applications. Development of fault-tolerant architectures is also needed because the number of defects increases inevitably as the component features shrink to the nanometre scale.

Such huge research effort has been devoted to the development and optimization of the CMOS platform that new technologies will first have to be compatible with CMOS. The main challenges are ensuring the practicality of integrating components based on widely differing technologies and materials, and introducing innovative schemes for cost-effective volume manufacturing

Finally, looking beyond the 2020 timeframe, new ideas and disruptive technologies need to be explored in order to create completely new computing devices capable that could eventually replace CMOS technology. This topic is discussed in more detail in ICT sector report "Beyond CMOS".

4. Applications and perspectives

The future of electronics will be smart multifunctional systems linked into networks and used in a variety of applications ranging from the personal (health care, wellness, information, information, communications, entertainment) to the public (energy, environment, mass transport, building). Nanotechnology is expected to have a significant and wide impact in the development of these applications.

This vision is closely linked to ambient intelligence: a future concept where intelligence is embedded in human environments in a user-friendly way. This assumes a shift in computing from desktop computers to a multiplicity of intelligent computing devices in our everyday lives. Mobility and seamless connectivity with other devices and fixed networks are essential enablers for ambient intelligence systems. This implies increased data rates which in turn requires more memory and computing power, and together with limited size leads to challenges with thermal management. The devices also need to be autonomous, robust and able to survive without explicit management or care.

Nanotechnology can provide solutions to several main constituents of ambient intelligence systems, such as sensing, actuation, radio, embedding intelligence into the environment, energy-efficient computing, memory, energy sources, human-machine interaction, materials and manufacturing. The key challenge lies in integrating these different functionalities to complete systems and finding solutions that allow cost-efficient mass manufacturing.

Due to the tremendously broad application scope, it is not cost effective to develop individual technologies for each application. Structured collaboration between the electronics sector and application sectors will enable enlarging existing markets (such as mobile communications, automotive), as well as speeding up the emergence of new markets (such as personal well-being, solid-state lighting).

The novel technologies that enable the functional enrichment in the 'Moore than Moore' domain also have strong interaction with 'Beyond CMOS' technologies. Although the R&D activities for carbon nanotubes and nanowires were initiated to address the future need of IC technologies beyond the physical limits of CMOS, an increasing effort is now devoted to using these technologies to create new functional products based on CMOS-compatible processes. A handful of products are already on the market, including CNT-based sensors, probe tips and transparent conductive films. In return, this increasing interest and broadening application opportunities will also benefit the long-term development of Beyond CMOS technologies.

5. Key players and experts (selection)

5.1. Industry Associations and Research Initiatives

ENIAC

The European Nanoelectronics Initiative Advisory Council (ENIAC) is the governing structure of the European Technology Platform - a bottom-up initiative that brings together leading European players in Nanoelectronics from industry, research and academia to develop and implement a coherent European vision and strategic agenda for this sector. ENIAC is working in close coordination with European and national public authorities and financial institutions, to implement its Strategic Research Agenda.

www.eniac.eu

ITRS

The International Technology Roadmap for Semiconductors (ITRS) is the fifteen-year assessment of the semiconductor industry's future technology requirements. It is sponsored by the five leading chip manufacturing regions in the world: Europe, Japan, Korea, Taiwan, and the United States. The objective of the ITRS is to ensure cost-effective advancements in the performance of the integrated circuit and the products that employ such devices, thereby continuing the health and success of this industry.

www.itrs.net

Semiconductor Research Corporation (SRC)

Semiconductor Research Corporation (SRC) is a research consortium that operates multiple research programmes both in the US and internationally. SRC programs include Nanoelectronics Research Initiative (NRI) (Beyond CMOS research).

<http://www.src.org/>

Semiconductor Equipment and Materials International (SEMI)

Global industry association serving the manufacturing supply chains for the microelectronic, display and photovoltaic industries

www.semi.org

6. References and Literature (selection)

The contents of this report are based on two main references:

ENIAC Strategic Research Agenda (update 2007),
<http://www.eniac.eu/web/downloads/SRA2007.pdf>

International Technology Roadmap for Semiconductors (ITRS), 2007 Edition, www.itrs.net

Additional sources of information:

ENIAC (European Nanoelectronics Initiative Advisory Council) website:
www.eniac.eu

Finnish ICT cluster nanotechnology vision work 2009 (organised by FinNano, the National Nanotechnology Programme of Finland), www.tekes.fi/eng/finnano

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