Technology Sector Report

Technology Analysis of Nanotechnologies for Data Storage

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1. Definition

This report examines nanotechnology-based approached to developing computer memory. The need for ever greater data storage capacities, across an increasing range of devices, with new requirements for size and resilience makes this a very interesting field of research.

1.1. Flash

The current dominant technology paradigm for most storage applications is flash memory. Flash is a type of Electronically Erasable Programmable Read Only Memory, or EEPROM. Flash employs memory cells in which two transistors are separated by an oxide layer. A cell sensor measures the charge in the floating gate, with high charge corresponding to a binary 1.

It has demonstrated consistent increases in storage capacity, whilst also being a durable and non-volatile. Most flash memory is now NAND-based, which means that access is only possible to blocks of memory (rather than true byte-level random access). It is also important to note that flash memory can involve sub-100nm feature sizes; in n 2006, Samsung announced NAND Flash memory of 64 GB with 40nm feature sizes. This employed charge-trap technology, rather than using metal single gate structures.

Flash suffers from two main challenges. The first is that memory performance degrades over time, with most Flash memory only lasting for 100 000 read/write operations. The other is than memory can only be erased a block at a time

1.2. Hard Disk Drives

For other storage applications, hard disk drives are used. These are rotating disks with magnetic surfaces, operating in a sealed environment. Storage capacity has increased, and devices have shrunk (currently the smallest hard disk drive is less than 1 inch in diameter).

These devices have moving parts, making them subject to mechanical failure due to either wear or shocks.

1.3. DRAM and SRAM

DRAM and SRAM are volatile memories, requiring power to maintain the contents of memory (DRAM also needs periodic refreshing of each memory cell). DRAM is the less expensive of the two types, but operates more slowly. Static RAM, in which a flip-flop holds each bit of memory is capable of operating at much higher speeds, but is also more expensive to produce. These memory types are more likely to be integrated onto a chip than used for general purpose storage.

2. Short description

There is a wide-variety of nanotechnology-based approaches to the development of memory:

- Magnetoresistive Random-Access Memory (MRAM)
- Programmable Metallization Cell (PMC)
- Phase-change Random Access Memory (PRAM)
- Resistive Random Access Memory (RRAM)
- Racetrack Memory
- Nanotube-based Random Access Memory (NRAM)

Many of the technologies that will be described are competing to become the ‘universal memory’ which exceeds the capacity, cost effectiveness of flash memory whilst maintaining its non-volatility, whilst also improving on the read/write speed of SRAM

2.1. Magnetoresistive Random-Access Memory (MRAM)

MRAM is believed to be one of the most promising approaches to develop a universal memory. MRAM consists of a fixed magnetic layer and a free magnetic layer, which are separated by a thin dielectric tunnel barrier. Each of these ‘sandwiches’ forms a single memory cell or magnetic tunnel junction. Each magnetic layer has a polarity, which can either be parallel (corresponding to one memory state) or anti-parallel. Polarity is persistent, rendering the device non-volatile.

To read this state information, an electric current is passed through the magnetic layers. If the layers have a parallel orientation, the resistance is lower than if they were to be anti-parallel. This change in resistance is the magnetoresistance of the name.

Wires run above and beneath the magnetic layers. These are aligned perpendicularly, creating a set of intersections at each memory cell. To write data, a current is passed through the cell which alters the polarity of the magnetic layers.

The most recent development of this technology is spin-torque MRAM, which uses electron spin to flip the magnetic field of the writeable layer. Normally the spin torque current must be applied for a sufficiently long time for several turns to take place, ensure reliable reversal of the field. German researchers at the Physical-Technical Federal Laboratory of Germany found that by adjusting the electric pulse used to reset the writeable layer, only a single wobble takes place. This would reduce write speed from ten to one nanosecond (corresponding to over 1 GHz write speed). However, these currents are currently unable to be supplied by current CMOS transistors.

This is an active area of research, and a number of companies are developing MRAM technology. Freescale Semiconductor has spun out its developments in this area to the company Everspin.

One of the challenges in the development of MRAM is that as quickly as it is able to demonstrate cost and performance improvements, it is still being outperformed by development of flash memory. In 2006, the cost of MRAM was reported to be approaching \$25/0.5MB, several orders of magnitude more expensive than flash memory at \$25/GB.

2.2. Programmable Metallization Cell (PMC)

This is a technology developed by researchers at Arizona State University, led by Dr. Michael Kozicki. The technology involves a thin film electrolyte sandwiched between one inert metal electrode, and one electrochemically active electrode. Each memory cell is written by applying a negative bias to the inert electrode, which ultimately results in the creation of a nanowire through the electrolyte. Where a nanowire is in place, the resistance is significantly lower, corresponding to a bit one state. To erase the cell, a positive bias is applying to the inert electrode.

Infineon, which has licensed this technology in 2004, refers to it as conductive-bridging RAM (CBRAM). NEC is also developing this technology under the title 'nanobridge'.

2.3. Resistive Random Access Memory

RRAM employs the ability to change the resistivity of certain materials; specifically that a dielectric material can be rendered conductive with the application of a sufficiently high voltage. This technology has a number of attractive features; the switching time is potentially quick (less than 10ns) and it may be possible to achieve storage densities of 100 Gbits/cm2.

Researchers at Hewlett-Packard discovered a fourth circuit element (after resistors, capacitors and inductors) called a memresistor, which could be applied as the storage media.

RRAM was also the technology domain pursued by the Nosce Memorias EU project, led by Paul Heremans of the University of Leuven. The major technology approach used by this project was the use of CuTCNQ, a metal-organic charge transfer material. Working life is a priority. This project was then followed by EMMA (Emerging Materials for Mass-storage Architectures).

2.4. Phase-change Random Access Memory (PRAM)

Also known as Phase Change Memory (PCM) and originally discovered by Stanford Ovshinsky at Energy Conversion Devices Inc. in the 1960s. PRAM uses the resistivity of chalcogenide glass as the storage media. Chalcogenide can exist in either crystalline or amorphous states. The amorphous state has high resistance and is used to represent 0, whilst the crystalline state has lower resistance and is used to represent 1. The chalcogenide alloy which is used is called GST Ge:Sb:Te (Germanium, Antimony and Tellurium). Crystallinity is lost at temperatures above 600C. The material is heated to change its state. Whilst the material does degrade, is does so at much slower rates than flash memory.

In 2006, Samsung announced a 512Mb PRAM memory with 47nm cell sizes. The device was marketed as having ten times the lifetime of flash memory, and being thirty times as fast. The company Numonyx, based in Switzerland, announced at the end of 2008 that it was commencing the supply of 128Mb PRAM memory. The product, named 'Alverstone' is produced on a 90nm CMOS fab.

One of the challenges of PRAM is that of ensuring reliable thermal phase change in different ambient temperatures.

2.5. Racetrack Memory

Racetrack memory is a technology developed by Stuart Parkin and colleagues at IBM. The possibility of storing information in magnetic domain walls had long been studied. Racetrack memory develops this with the use of permalloy nanowires as a magnetic material to store information.

A spin polarized current interacts with the magnetization of the domain walls to provide torque, and therefore is able to move magnetic domains along a permalloy nanowire ‘track’. A magnetic tunnel junction is then used as a sensing element to read data from the racetrack nanowires.

A number of related research activities are underway. Guido Meier at the University of Hamburg has carried out work which finds that movement of domains can be impaired by imperfections in the crystal.

It may also be possible to align the wires vertically above the read-write head, resulting in 3D memory.

2.6. NRAM®

NRAM is registered trademark of Nantero, and is alternatively defines as either nanotube-based or non-volatile RAM. Suspended nanotube junctions are used as memory bits. Nanotubes are suspended above an electrode, corresponding to a bit zero state. When voltage is applied, the nanotube will be pulled towards the electrode. This corresponds to a bit one state. This is non-volatile memory, as the nanotube will be either suspended in the zero state mechanically, or will be held in the on state due to the Van der Waals force.

This technology was invented by Thomas Rueckes, currently Nantero's Chief Technology Officer, whilst a research fellow at Harvard.

3. Additional demand for research

3.1. Cell Size

The cell size affects the storage density of the memory, expressed in measurements like Gb/inch. Some issues with MRAM include the challenge that as memory cell sizes shrink, the current used to change the polarity of the writeable layer can also affect surrounding cells. An approach to addressing this is the ‘toggle mode’.

3.2. Cost

Existing technologies like flash are still able to demonstrate decreasing costs per unit of storage. To supplant existing technologies in mass market applications, nanotechnology based approaches will need to demonstrate increasing cost-effectiveness. The cost of MRAM in 2006 was reported to be $25/0.5MB, versus Flash at $25/GB.

The cost of new technology approaches is mainly related to their manufacturing requirements. Those technologies that can be created using standard CMOS fab stand a better chance of being cost-effective.

4. Applications and perspectives

Mass storage is a largely commoditised market with rapidly increase cost/per storage unit. In the first instance, many of these novel approaches to data storage are better suited to applications with more specific technical requirements, in which cost is less of a factor.

These may include applications on embedded devices, or those in which high resilience to electromagnetic radiation needs to be demonstrated. MRAM may be used for datalogging-specific memories (black boxes), in which resilience is important. There are also some on chip applications, such as write buffers which require high density but lower speed storage. Freescale's MRAM product has been used in satellite applications, in which radiation levels render current approaches impossible.

5. Key players and experts (selection)

5.1.1. Projects, Industry Associations, etc.

- Probe-Based Terabit Memory (ProTeM), http://www.protem-fp6.org/
  (Coordinated by the University of Exeter, UK, this project is developing probe-based terabit memory)
- Advanced Technology for Holographic Storage (ATHOS), http://www.athos-holography.net/
- ChAlcogenides MEmories for multiLevel Storage (CAMELS), http://www.ist-world.org/ProjectDetails.aspx?ProjectId=832189bb8e2c4b378e05f41e7b97c6a6&SourceDatabaseId=7cff9226e582440894200b751bab883f
- Emerging Materials for Mass Storage Architectures (EMMA), http://www.imec.be/EMMA/
- Nosce Memorias, http://www.imec.be/NosceMemorias/Home.html
  (This Project ended in 2007)

6. References and Literature (selection)

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Spin flip trick points to fastest RAM yet (2008), New Scientist, http://www.newscientist.com/article/dn14525-spin-flip-trick-points-to-fastest-ram-yet.html?feedId=online-news_rss20

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