



Economic Analysis of Nanotechnology for ICT

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1. Executive Summary

In Europe, the value of the ICT industry is around 8% of Europe's total GDP. 6% of the European workforce is employed in ICT-related fields¹. ENIAC reported that the global market for electronics was US\$1340bn in 2005, with the value of semiconductors alone at US\$265bn. This share of European employment equates to about 13 million jobs.

Electronics will be one of the industries upon which nanotechnology will have the most sustained, significant impact, as so much of the technology development in this area is scaling to (or is already at) nanometre length scales.

This report considers four of the major applications for nanoelectronics and photonics: Integrated circuits, Electronics manufacturing equipment, Displays, and Data storage.

Nanotechnology for integrated circuits may lead to improvements in processor density and performance, energy efficiency and reliability. Many of the applications of nanotechnology for integrated circuits will only be realised in the mid – to long term. In terms of current applications, Intel is believed to use an atomic layer deposition process to deposit high-k materials in the fabrication of 45 nm chips

Creating integrated circuits with smaller feature sizes is likely to involve improvements to existing manufacturing technologies, and the introduction of new techniques. Some of these technologies, such as atomic layer deposition and nano-imprint lithography are largely novel, nanotechnology-based approaches. Tools based on these approaches are commercially available.

There are three main groups of nanotechnology-enabled display technologies; Organic Light Emitting Diodes (OLED), Field Emission Displays (FED), and Surface-conductive Electron-emissive Displays (SED). FED/NED and SED displays are not currently commercially available. OLED displays are commercially available, albeit largely restricted to portable electronic applications such as mobile phone screens and laptops. iSuppli states that the current OLED market size is around US\$ 500, with over 80 000 units shipped in 2008².

¹ http://ec.europa.eu/enterprise/ict/index_en.htm

² <http://www.isuppli.com/Abstract/ABSTRACT%20-%20OLED%20Market%20Tracker%202008.pdf>

There are a number of nanotechnology-based approaches to the development of data storage; Magnetoresistive Random Access Memory (MRAM), Ferroelectric RAM, (FeRAM), Resistive RAM (RRAM), and NRAM (Nanotube RAM). A 2005 study by NanoMarkets projected that nanotechnology-enabled storage devices would be a \$65,7bn market by 2012³; accounting for 40% of the total memory market.

³ NanoTechWire, <http://nanotechwire.com/news.asp?nid=1059&ntid=123&pg=11>

2. Methodology

2.1. Definition

For the purposes of this report, nanotechnology is defined as “the study of phenomena and fine-tuning of materials at atomic, molecular and macromolecular scales, where properties differ significantly from those at a larger scale.”⁴

2.2. Methodology for Preparing the Report

The development of this report has been a three stage process. Desk research using publicly available sources of information was used to produce a first version of this report. Input and feedback is then sought from experts, via questionnaires, interviews and discussions, and from the ObservatoryNano symposium which takes place in March 2009. A final report is then produced, which synthesises the desk research and external expert input.

2.3. Methodology for Quantitative Assessment

Quantitative assessments of market size, growth rates, and the current market shares of nanotechnology enabled products are developed using external data sources such as market research providers, industry groups, and individual experts. Estimates and market size projections that are made by the authors of this report are clearly marked as such.

All forward looking estimates are necessarily a projection, and are therefore subject to error within the market models themselves, as well as to unforeseen external events. In particular, the current economic crisis has forced countries and companies to significantly adjust their growth forecasts – in most cases, this will not have been taken into account in projections which date from before 2008.

⁴ Introduction to Nanotechnology, http://ec.europa.eu/nanotechnology/index_en.html

3. General Market Description

3.1. Brief Market Description

In Europe, the value of the ICT industry is around 8% of Europe's total GDP. 6% of the European workforce is employed in ICT-related fields⁵. ENIAC reported that the global market for electronics was US\$1340bn in 2005, with the value of semiconductors alone at US\$265bn. This share of European employment equates to about 13 million jobs – which includes a number of activities related to the development or use of ICT (such as software development), but which are not directly linked to the manufacture of electronic devices.

The largest companies in this sector are based in the United States or Asia. Fortune magazine's Global 500 ranking of the world's largest corporations by revenue lists eight ICT companies (Samsung, Hewlett-Packard, IBM, Hitachi, LG, Matsushita, Sony) before coming to the first European representative – Nokia, in 88th position. Other European ICT companies in this listing include Ericsson and Phillips⁶. The revenues of other European companies are too low to appear on this list, but are nonetheless substantial companies (ST Microelectronics, 2008 revenue US\$ 9.84B; Infineon Technologies, €4,321M, and ASML, €2,9M).

Companies involved in this industry range from large, integrated suppliers of computing equipment and related services (such as IBM); to manufacturers of particular component types like memory or displays. In general it is a highly competitive industry, with rapid technological development and relentless pressure on price and performance.

Improvements in ICT also have societal benefits. As the recent “Strategy for ICT R&D Innovation in Europe”⁷ states:

ICT is also essential to address Europe's societal challenges. It brings unique responses e.g. to the growing needs for sustainable healthcare and ageing well, for better security and privacy, for a lower carbon economy and for intelligent transport.

⁵ http://ec.europa.eu/enterprise/ict/index_en.htm

⁶ <http://money.cnn.com/magazines/fortune/global500/2008/index.html>

⁷ http://ec.europa.eu/information_society/tl/research/documents/ict-rdi-strategy.pdf

3.2. Nanotechnology Impact

Electronics will be one of the industries upon which nanotechnology will have the most sustained, significant impact, as so much of the technology development in this area is scaling to (or is already at) nanometre length scales.

3.2.1. More Moore

Moore's Law, coined by Intel's Gordon Moore, states that transistor density on a processor will double every two years. As the size of the processor itself remains fairly constant, this means that more and more transistors need to fit into ever smaller spaces. Intel's latest generation of chips, Penryn and Nehalem, have 45nm feature sizes and in a quad-core configuration have over 731 million transistors⁸.

Moore's Law was intended to be a function of size and cost; the number of transistors would not only be function of the number that could physically fit on the chip, but that this would also be at the optimal price point, beyond which defect rates and other factors would increase the cost of the chip.

This scaling of features cannot continue indefinitely. Already the lithography process by which silicon chips are fabricated has had to change to reflect the fact that feature sizes are smaller than the wavelength of light – visible light has wavelengths down to 380nm, and so Extreme Ultraviolet (10nm) is increasingly being used. Eventually quantum effects will be seen, in which electrons pass through barriers of 1nm, despite not normally having sufficient energy to do so.

In terminology widely used by the electronics industry, nanotechnology which leads to continued miniaturization belongs to the More Moore technology domain. Whilst this does involve working with nanometre length scales, it is often considered that this is not true nanotechnology, as the main task is scaling existing processes. Novel processing methods, such as self-assembly, belong to the Beyond CMOS domain.

⁸ [http://en.wikipedia.org/wiki/Nehalem_\(CPU_architecture\)](http://en.wikipedia.org/wiki/Nehalem_(CPU_architecture))

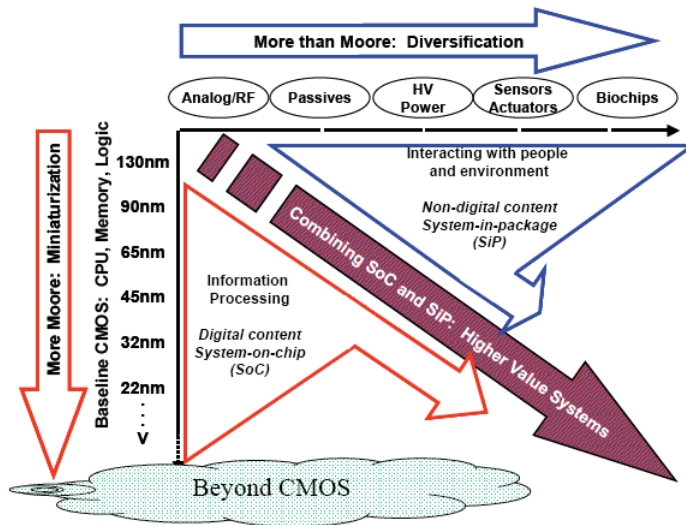


Figure 1: Moore's Law and More⁹

3.2.2. Beyond CMOS

The Beyond CMOS domain refers to a set of disruptive functions that, in the long term, will complement or replace conventional silicon technology. The novel devices should show significant advantage over the “ultimately scaled” CMOS transistors in power, performance, density, and/or cost to enable the semiconductor industry to extend the historical cost and performance trends for information technology.

Two main approaches are used to develop technologies that would extend the functional scaling in the 2020 or beyond timeframe. One is heterogeneous integration of new technologies with the CMOS platform (functional diversification – see next section “More than Moore”). The second is to develop fundamentally new approaches to information processing.

Nanotechnology will enable developing alternative schemes to encode and process information in order to discover a new mechanism for computing that goes beyond simply improving today’s transistor. For a large part, future information processing will be done on information where the state variable is something other than electronic charge. This information includes optical images,

⁹ <http://www.itrs.net/Links/2007ITRS/ExecSum2007.pdf>

image sequences, speech, and data sets derived from physical sensors. Alternative options for new information carriers include e.g. spin, molecular state, photons, phonons and quantum state.

Nanotechnology will also develop new methods of processor manufacture, including nanoimprint lithography, printed electronics and even self-assembly. These technologies have the potential to displace existing silicon CMOS fabrication methods, and reduce the requirement for multi-billion Euro manufacturing facilities. Before doing so, these methods will need to demonstrate the cost-effectiveness and reliability currently demonstrated by Silicon CMOS.

3.2.3. More than Moore

Nanotechnology is believed to also have a significant impact on the development of other functional components beyond processors and memory.

Nanophotonics, the control of light at sub-wavelength scales, is one of the most promising areas of nanotechnology development, with applications across a wide range of sectors. The technology domain includes 1 dimensional, 2D, and 3D nanostructures, quantum dots, metamaterials which demonstrate negative refraction, plasmonics, and a number of other research areas.

Applications for nanophotonics include displays, lighting, optical data communication and interconnection, as well as photovoltaics, sensing, and imaging/instrumentation. Europe has an active photonics area, including both large industrial players (such as Philips, Osram, Thales) and newer companies, often spun out from research centers.

Nanotechnology advances in displays can be divided into two broad categories; those which rely on the field emission properties of nanostructured materials (such as Field Emissive and Surface Emissive Displays) and those which involve the use of new materials and patterning technologies to allow the use of organic layers and/or flexible substrates.

New memory technologies enabling exponentially higher storage capacities will also be enabled by nanotechnology. A wide range of technologies is being considered, including MRAM, FeRAM and phase change memory.

Because of the importance of nanotechnology for electronics, almost every major manufacturer has research activities in one form or another. The largest European initiative is the Nano 2012/ Crolles3 programme, funded by the French government with approximately €457M, and with

STMicroelectronics as the main corporate partner¹⁰. IBM and Hewlett-Packard have some of the most productive nanotechnology research, having recently been responsible for the development of racetrack memory and the memresistor, respectively.

Developments in nanotechnology for ICT will also have an effect on the countless industries in which ICT plays an important role. To take a seemingly trivial example, miniaturisation of memory enabled the development of the iPod, which in turn has had a significant impact on the music industry, changing it from being a producer of physical products (CDs) to digital goods.

3.3. Drivers and Barriers to Innovation

As has been mentioned, the electronics industry is highly competitive and demanding of continuous performance improvements. This means that the electronics industry has a high propensity for innovation. Of the 20 global firms that spend most on R&D, six are in the electronics sector (Nokia, Samsung, IBM, Intel, Matsushita and Sony). Combined, these firms spent 35bn USD on R&D in 2007.¹¹

Electronics firms have also been the largest industrial funder of nanotechnology research, investing US\$2.88bn in 2006, accounting for 54% of total industrial investment¹². This is indicative of the extent to which so much electronics research and development extends into nanotechnology domains.

3.3.1. Drivers of Innovation

One of the major drivers of innovation is that the highly competitive electronics marketplace spurs continuous product improvements, in order to eke out competitive advantage, however temporary. Exponential development is seen in areas of electronics beyond integrated circuits, with dramatic increases in data storage density, for example.

Cost reduction is another driver, though it is worth noting that this could also be seen as a barrier. New technology approaches, unless they demonstrate dramatically enhanced performance, are

¹⁰ http://www.eetasia.com/ART_8800561610_480200_NT_ded29556.HTM

¹¹ Beyond Borders: The Global Innovation 1000, Booz Allen Hamilton, http://www.strategy-business.com/media/file/sb53_08405.pdf

¹² Lux Research, The Nanotech Report 5th Edition

unlikely to gain market share until they become cost competitive with existing approaches. Cost drivers can be seen in areas such as CNT thin film transistors, in which one of the drivers is to replace an expensive material input, Indium Tin Oxide.

Changing end-user needs provide an impetus for innovation. As the ENIAC SRA argues, ICT is being incorporated into a wider variety of domains, including healthcare, transport, and security. These new applications require different technologies.

3.3.2. Barriers to Innovation

A number of features of ICT drive innovation and development in other industries in turn. However, that is not to say that there are no barriers to innovation in ICT – they exist, and at both global and regional levels.

For one, the investment that has been sunk into CMOS research, process development, and fabrication facilities gives rise to path dependency – companies would rather prioritise R&D activities that prolong the life of CMOS (a rational economic strategy). This is clearly a factor in deciding where to allocate resources, and one which becomes even more acute in challenging economic times. However, it has not seemed to prevent companies in this space from considering more future orientated nanotechnology research.

The dominance of the CMOS paradigm is also indicative of the highly (and continuously) optimised state which it has reached. To supplant this for semiconductor production and alternative technology would need to demonstrate cost effectiveness, low fault tolerance, and high throughput reliability across billions of produced units.¹³

¹³ ENIAC SRA

The report “Shaping the ICT Research and Innovation Agenda for the Next Decade”¹⁴ identified several potential barriers to the development of an ICT supply industry in Europe. The three most important were found to be:

- Weak public financial support for R&D
- Market fragmentation
- Lack of world-class research and innovation clusters

‘Weak public financial support for R&D’ refers not only to direct public funding of ICT, but also the ways in which the public sector can support ICT development indirectly. One lever available to the public sector to stimulate ICT development, public procurement, is more heavily utilised in the United States. The current European level of pre-commercial ICT procurement is at €1bn, one tenth of the US figure.¹⁵

Market fragmentation increases the complexity of innovation and business activities, and refers specifically to there being a very large number of potential customers, operating within differing local market structures, conditions and regulations.

The point that Europe was lacking world-class research and innovation structures drew a polarized response in regard to micro-nano electronics; 23% felt that Europe was strong in this area, whilst 24% felt that Europe was weak. It is certainly the case that a number of initiatives including ENIAC, and the new European Commission ICT strategy published in March 2009¹⁶, intend to develop European research excellence in ICT.

3.4. Relevant Sector Segmentation and Applications

This report considers five of the major applications for nanoelectronics and photonics:

¹⁴

http://ec.europa.eu/enterprise/newsroom/cf/document.cfm?action=display&doc_id=2086&userservice_id=1&request.id=0

¹⁵ http://ec.europa.eu/information_society/tl/research/documents/ict-rdi-strategy.pdf

¹⁶

<http://europa.eu/rapid/pressReleasesAction.do?reference=IP/09/397&format=HTML&aged=0&language=EN&guiLanguage=en>

- Integrated circuits
- Electronics manufacturing equipment
- Displays
- Data storage
- Optical interconnects.

This correlates closely to the technology area sector segmentation in the ObservatoryNano technical reports. Typically each of these applications then has a very wide range of end-user uses – in the case of integrated circuits; for example, there are a very large number of devices that utilise an IC in some way.

3.5. Possible Future Products and Time Range

This timeline summarises the product introduction timelines that are discussed within each application sector.

Application	Commercially Available	1-3 years	3-5 years	5+ years
Integrated Circuits	ICs with 45nm features (Intel)	Continued shrinking of feature sizes		Beyond CMOS ICs
Manufacturing Technologies	Atomic Layer Deposition Nano Imprint Lithography stamps			
Displays	OLED displays, up to 13”	CNT thin films. SED displays Larger OLED displays	FED displays	
Memory	MRAM modules FeRAM	Continued development of MRAM	Phase Change Memory, Resistive Random Access Memory	Racetrack Memory
Photonics	Optical Interconnects			

4. Application Profiles

4.1. Integrated Circuits

The classic definition of an integrated circuit is ‘an electronic circuit where all the elements of the circuit are integrated together on a single semiconductor substrate.’¹⁷

4.1.1. Short application description

During the last decades, the smallest pattern sizes on silicon wafers have been reduced from 6 - 8 microns to around 20 nanometres. Similarly, manufacturing relied on 25-mm diameter wafers, whereas today it's done on 300 mm wafers. New technology generations continue to be introduced every 2-3 years. At the same time, the number of technical challenges increases. In addition to geometrical scaling, material and architecture innovations will play a more important role in the future to enable further increases in device performance. By combining silicon innovations with other novel nanotechnologies, it is expected that Moore's Law will extend well into the next decade (until 2015).

Continuous size reduction of CMOS transistors (the basic building blocks of logic circuits) has produced enhanced performance for decades in terms of speed, power consumption, reliability and cost per function. Now significant challenges are expected. The conventional path of scaling, which was accomplished by reducing the gate dielectric thickness, reducing the gate length, and increasing the channel doping, might no longer meet the application requirements set by performance and power consumption. Introduction of new material systems as well as new device architecture, in addition to continuous process control improvement are needed to break the scaling barriers.

4.1.2. Functional requirements

Continuous size reduction of CMOS transistors (the basic building blocks of logic circuits) has produced enhanced performance for decades in terms of speed, power consumption, reliability and cost per function. Although Moore's law was initially made in the form of an observation and forecast, it became to be accepted as a goal for the entire industry.

¹⁷ <http://www.icknowledge.com/glossary/i.html>

Almost 70% of the total semiconductor components market is directly impacted by the miniaturization trend. This 70% comprises three component groups of similar size: microprocessors, mass memories, and digital logic.

Processor density

Moore's Law states that the number of transistors on a chip doubles about every two years. New technology generations continue to be introduced every 2-3 years. Intel's 45 nm logic technology is currently in production and, according to Intel, the delivery for the next 32 nm technology generation is on target.

Processor performance

The speed of the world's most powerful computers has increased exponentially, doubling about every year and a half in line with Moore's Law. That's an increase of roughly a factor of 10 every five years. Further increase in processing performance will enable new computing applications, such as real-time language translation or facial recognition.

High-performance computing has also fundamental impact on science and engineering. Computer simulations will open the way for discoveries in areas where analytic theory and experimental science are insufficient alone. This is particularly important for areas such as nanotechnology where experiments are often very difficult and costly to conduct.

Energy efficiency

The rising transistor count and their smaller size (increased speed) also lead to increased power consumption. Consequently energy efficiency is becoming increasingly important. Instead of measuring gigahertz rates, the semiconductor industry is now focusing on performance-per-watt (high-speed, low-power transistors). Energy efficiency is also linked to thermal management, an issue which has been defined as one of the most critical research topics to create future computing devices.

Reliability

Another significant challenge is reliability. As computer size grows, the components need to be more reliable or have more redundancy and fault tolerance. In general, the number of fabrication flaws is unavoidably increasing as the circuits shrink towards the nanometer scale. Many nanoscale devices simply do not work as expected or occasionally are broken or shorted together.

4.1.3. Boundary conditions

While it is foreseen that it is possible to continue the development of CMOS technology well into the next decade, economical limits to device scaling could be reached even before that. Keeping up with Moore's Law requires major investments continuously from all players in the value chain. For each new process technology generation, the costs increase. As a result, only a few players globally can produce sufficient R&D mass.

Moreover, developing new disruptive technologies in the Beyond CMOS domain will require even much greater capital input. For this reason, new technologies will first have to be compatible with the CMOS platform.

There is also a growing amount of new technology options available and a rapidly growing diversity of required materials, while the initial markets can be very fragmented. This makes it very difficult to bridge the gap between innovation and future volume markets.

4.1.4. Product examples

Hafnium-based Intel® 45nm Process Technology

Intel's new 45nm high-k metal gate silicon technology uses new materials including hafnium to replace the transistor's silicon dioxide gate dielectric and new metals to replace the polysilicon gate electrode. The new technology helps to reduce electrical leakage and thus enables smaller, more energy-efficient and higher-performance processors.

4.1.5. Economic Information and Analysis

Many of the applications of nanotechnology for integrated circuits will only be realised in the mid – to long term. In terms of current applications, Intel is believed to use an atomic layer deposition process to deposit high-k materials in the fabrication of 45 nm chips. The new materials along with the right process technology are the key enablers in extending the scaling of silicon technology to 45 nm and beyond. However, estimating a value of nanotechnology impact, in terms of its overall contribution to the value of the finished chip, would be almost impossible to do accurately.

4.1.6. Selected Key Companies Profiles

Intel

Intel (<http://www.intel.com/>) is the world's largest semiconductor manufacturer, with 2008 revenues of USD 37.6 billion. The company carries out extensive work on IC design and production process optimisation.

NXP

NXP (<http://www.nxp.com>) was established as an independent company in 2006, having previously been the semiconductor arm of Phillips. The company recorded revenues of USD 5.4 billion in 2008.

STMicroelectronics

STMicroelectronics (<http://www.st.com>) is a semiconductor company with 2008 sales of USD 9.8 billion. The company has a broad product portfolio, producing for mobile, computer, industrial and automotive applications.

Infineon Technologies

Infineon (<http://www.infineon.com>) produces ICs and systems for industrial, automotive, security and communications applications. The company's 2008 revenues were around EUR 4 billion.

4.2. Manufacturing Technologies

4.2.1. Short application description

Creating integrated circuits with smaller feature sizes is likely to involve improvements to existing manufacturing technologies, and the introduction of new techniques. Some of these technologies, such as atomic layer deposition and nano-imprint lithography are largely novel, nanotechnology-based approaches. Other approaches – extreme ultraviolet lithography (EUVL) – employ nanometre wavelengths but don't fit the classic definition of nanotechnology. For a more detailed description of the technologies in this field, please refer to the technology sector report 'Manufacturing Technologies'.

The primary application is the manufacturer of electronic devices. This includes the fabrication of integrated circuits, memory elements, and other electronic components. Electronics has very demanding manufacturing environments, requiring high throughput, low defect rates, cost effectiveness – rather than low cost per se – and the ability to produce nanometre scale features on devices which then be integrated in larger systems.

The manufacturing process for an integrated circuit includes the following process steps¹⁸:

1. A layer of silicon dioxide is grown on a wafer
2. The wafer is coated with a photoresist
3. UV light is then used to pattern the wafer, with a mask shielding parts of the photoresist
4. The photoresist that has been exposed to UV light is dissolved
5. The silicon dioxide which is then uncovered is etched away
6. The rest of the photoresist is then removed, leaving a silicon dioxide pattern.
7. The process is then repeated to create another layer of features
8. Exposed areas are then doped
9. Further layers are created, with an IC typically consisting of 20 or more.

This is a simplistic description, but it illustrates the main elements; deposition of a material (such as Silicon Dioxide), patterning, etching and doping.

¹⁸ <http://www.intel.com/education/makingchips/>

Atomic Layer Deposition is believed to be employed in the deposition phase of Intel's manufacturing process, in order to create high-k/metal gate dielectrics.

Nano Imprint Lithography is being considered to produce the insulating layers that are required to separate copper interconnects between transistors, and has been added to the 32 and 22nm nodes on the International Technology Roadmap for Semiconductors.

4.2.2. Functional requirements

Resolution

The resolution of a manufacturing technology refers to the feature sizes that can be patterned using this technology. Recalling that Intel currently produces integrated circuits with 45nm feature sizes, any new technology would need to demonstrate higher resolution (or vastly reduced costs). Nanoimprint lithography has used stamps with xxx feature sizes.

Defect Rate

Defect Rate, typically measures as defects per square cm. Integrated circuit manufacturing is high defect intolerant, with a defect rate of xx leading to the rejection of the wafer. Other applications – such as the production of Flash memory – can be more tolerant to defects.

A number of factors can be responsible for the introduction of defects in the manufacturing process. The chemicals used to produce a device may leave contaminants on the wafer surface. The technology may also result in positive charging of the wafer, leading to a risk of electrostatic discharge.

Throughput

In semiconductor fabrication, this is typically a measure of the number of the wafers than can be processed per hour. Production Nano Imprint Lithography systems from Obducat are capable of processing up to 30 wafers per hour, with an imprint area of 8”¹⁹.

¹⁹ <http://www.obducat.com/Default.aspx?ID=489>

4.2.3. Boundary conditions

In essence, the boundary condition is defined by the existing technology, on a combination of metrics. The overall production cost should be lower than an existing method, cost being a function of the production time and throughput, the defect rate, material and equipment requirements.

4.2.4. Product examples

Sindre[®] 800 Nano Imprint Lithography System

Obducat's largest production NIL system includes process steps for applying the imprint stamp with consistent pressure, thermal or UV curing, and the use of polymer replicas of the master stamp, increasing the master's lifetime.

SUNALE[™] P-SERIES ALD Process Tools

Picosun's P-series reactors are designed for production use, processing batches of 25-50 4" wafers. The reactors can be used for a wide variety of applications, including optoelectronics, MEMS, and semiconductor materials.

4.2.5. Economic Information and Analysis

A 2006 report by BCC Research gave the market value of nanopatterning tools and equipment at US\$ 46.3 million, of which 74% was accounted for by Nano Imprint Lithography. The market value was project to rise to US\$ 292.7 in 2010, the bulk of which (84%) would continue to be NIL²⁰. The largest single market was in semiconductor and electronic fabrication applications.

Another 2006 report by BCC gave the market value of ALD at US\$ 214.1 million in 2005. This whole market figure included equipment, as well as materials.²¹

²⁰ <http://www.bccresearch.com/report/NAN041A.html>

²¹ http://www.electronics.ca/reports/materials/ald_market.html

4.2.6. Selected Key Companies Profiles

Obducat

Obducat (<http://www.obducat.com>) was the first commercial provider of NIL equipment, having sold the first NIL machinery in 2001. The company is based in Sweden and is listed on the Nordic Growth Market. In addition to the production of NIL equipment, Obducat also sells Electron Beam Recorders (EBR) which are used to fabricate the master stamp.

Molecular Imprints

Molecular Imprints (<http://www.molecularimprints.com/>) also sells patterning lithography equipment, under the trademark Step and Flash® imprint lithography (S-FIL®). The company's largest system, the Imprio® HD2200, produces 20nm pitch sizes with a throughput of 180 disks per hour.

NIL Technology

NIL Technology, based in Denmark, fabricates nanolithography stamps and associated processing and consultancy services.

Beneq

Beneq (<http://www.beneq.com>) based in Finland, is a provider of coating technologies, including ALD. The company has three reactor products for thermal and plasma ALD.

Picosun

Picosun (<http://www.picosun.com>) sells Atomic Layer Deposition systems. Tuomo Suntola, the inventor of ALD, is a member of the board of Picosun.

Other companies include Cambridge Nanotech (<http://www.cambridgenanotech.com/>), ASM International (<http://www.asm.com/>), Nanonex (<http://www.nanonex.com/>)

4.3. Displays

4.3.1. Short application description

There are a wide range of displays applications, the most ubiquitous being displays for portable electronics; such as computers and mobile telephones; and televisions. The current dominant technologies are liquid crystal display (LCD) and plasma display panel. Cathode Ray Tube (CRT) displays are increasingly being phased out in favour of these new technologies.

Graduations of screen sizes range from 1” or 2“ to 3.5” for mobile devices, 12”-17” for laptop computers, and 19” to 70” for televisions. Typically all devices would be full colour, and with the exception of older screens for mobile devices, would be capable of showing full motion video.

There are three main groups of nanotechnology-enabled display technologies that are relevant for this application:

- Organic Light Emitting Diode (OLED), in which the emissive layer is an organic compound
- Field Emission Display (FED), in which an element such as a carbon nanotube acts as an electron source, striking a coloured phosphor
- Surface-conductive Electron-emissive Display (SED), which is similar to FED in many ways, the difference being that it only employs a single field emitting element – which could also be a CNT – per pixel.

The technology behind each of these approaches is described in more detail in the Technology Analysis section.

4.3.2. Functional requirements

The function requirements of displays include:

Refresh rate

A measure of how often the display refreshes the image that it is displaying – in CRT displays, this was the length of time taken for the cathode ray tube to scan across each pixel. A display with a slow refresh rate may appear to flicker. The refresh rate (or response rate) for LCDs is determined by the amount of time it takes to instruct each liquid crystal to change its state. A

commonly used refresh rate is 60Hz, but higher rates (which are a multiple of 24, the number of frames per second in video film) will reduce the sensation of ‘judder’ or motion blur.

Viewing Angle

LCD displays can be difficult to view at oblique angles – an effect which can easily be seen on a laptop computer screen. The viewing angle determines a ‘cone of visibility’ extending from the display, within there is sufficient contrast for a person to view the image being displayed. A narrow viewing angle restricts some applications for televisions and displays.

Power

The power consumption of a display is particularly important in battery-powered mobile devices; within with they can be a major source of power consumption. LCDs have typically been considered to have higher power requirements than alternative display technologies, due to the requirement that they be backlit (and with part of this light then being blocked by a polarising filter).

Contrast Ratio

The contrast ratio of a device describes the ratio between the light intensity of the lightest part and the darkest part of the display. Taken in isolation, a higher contrast ratio should give a better display performance. Improvements to contrast ratios have been one of the selling points of OLED displays, which claim contrast ratios of 1 000 000:1 (LCD displays would typically have a contrast ratio of 5 or 10 000: 1). The noticeable effect for a viewer is that the black areas of an OLED display appear to be true black, whereas in an LCD they would be very dark grey.

Lifetime

A display’s lifetime is often expressed as the time it will take for a display to lose half of its brightness, and is measured in hours. 60 000 hours is considered typical for LCD and Plasma displays. OLEDs have had particular challenges in longevity, as organic materials used have a tendency to degrade – this is a priority area in OLED research.

4.3.3. Boundary conditions

There are a set of very basic boundary conditions which apply in the market for device displays and television; that the device is capable of showing moving, colour images – whilst the major technologies described here do this, flexible displays are restricted to images which change far more slowly than 24 frames per second.

4.3.4. Product examples

Sony XLE 1

Sony's XLE 1 is an OLED digital TV²², and is currently commercially available. The screen size is 11" – OLED laptop displays of similar dimensions are also commercially available, though larger sizes that would be more suitable for televisions are not, as yet.

The XLE 1 is sold on its image quality and thinness (it is 3mm wide), though the product itself is relatively expensive at US\$ 2499 – several times more expensive than much larger LCD and Plasma displays.

Nanospindt FED (Sony / FE Technologies)

A 19" FED was demonstrated at a number of events in 2008, showing an input from a high definition source (a Playstation 3). Coverage of the display cited a distinct lack of motion blur and true black, making for an impressive visual performance.

Toshiba SED

Toshiba first demonstrated an SED display in 2006, and it was then announced that commercial SED products would ship in the latter half of 2007. These were to have been targeted for

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<http://www.sonystyle.com/webapp/wcs/stores/servlet/ProductDisplay?catalogId=10551&storeId=10151&productId=8198552921665327724>

profession users such as TV studios – an application in which the demand for high quality colour reproduction renders the users less price sensitive²³.

However, the technology was then the subject of a lengthy legal wrangle between Toshiba, Canon, and Applied Nanotech Inc. Canon and Toshiba had formed a joint venture named SED Inc. Applied Nanotech subsequently sued Canon, alleging that they had violated a confidentiality agreement by sharing information with Toshiba. SED Inc. then became a wholly owned subsidiary of Canon in 2007²⁴. Applied Nanotech ultimately dropped their lawsuit in December 2008, enabling Canon to resume production of SED displays. Uncertainty remains as to the amount of development Canon was able to carry out during this period, and how close to market this technology now is.

Motorola Nano Emissive Display (NED)

Motorola demonstrated a 5” prototype NED in May 2005 with full colour video and a thickness of 3.3mm. The NED is believed to be Motorola’s term for what is more generally understood to be a FED. Since this release, no more information has been forthcoming about Motorola’s development of this technology.

4.3.5. Economic Information and Analysis

FED/NED and SED displays are not currently commercially available. Assuming that Canon resumes work on their SED; this is likely to be first to market in 2009/10.

OLED displays are commercially available, albeit largely restricted to portable electronic applications such as mobile phone screens and laptops. iSuppli states that the current OLED market size is around US\$ 500, with over 80 000 units shipped in 2008²⁵. Analysts Display

²³ http://techon.nikkeibp.co.jp/english/NEWS_EN/20061225/125850/

²⁴ <http://www.canon.com/press/2007/sed2007jan12.html>

²⁵ <http://www.isuppli.com/Abstract/ABSTRACT%20-%20OLED%20Market%20Tracker%202008.pdf>

Search predict that OLED displays will account for 5% of the display market by 2015 (the proportion currently being around 1%)²⁶.

4.3.6. Selected Key Companies Profiles

Canon

As of 2007, Canon wholly owns the assets of SED Inc., a joint venture established by Canon and Toshiba to develop Surface-conduction Electron-emitter Displays. Canon does not currently sell televisions or displays, but they are incorporated into the company's products, including camcorders and digital cameras.

Sharp

Sharp is a Japanese electronics manufacturer with 2008 sales of US\$ 35.5 million.²⁷ Audio-visual equipment – including LCD colour televisions – accounts for 39.4% of total sales. LCD modules for other devices, such as mobile phones and computers, are a further 30.5% of Sharp's annual sales. The company's research work includes further improvements to LCD technology, and the inclusion of optical sensors to record user input (as an alternative to touch screens).

FE Technologies (<http://www.fe-tech.co.jp/en/index.html>)

FE Technologies is developing FED technology under the product name 'nano-Spindt'. The company is a spin-out from Sony, and continues the research and development that was carried out by that company.

²⁶

http://www.displaysearch.com/cps/rde/xchg/displaysearch/hs.xsl/090219_oled_display_revenues_expected_to_reach_6b_in_2015.asp

²⁷ <http://sharp-world.com/corporate/ir/library/annual/index.html>

Motorola

Motorola released a 5” NED prototype in 2005. At this point the company claimed to have over 150 patents “in CNT and flat panel displays”. No information about the company’s NED has been available since this point.

4.4. Data Storage

4.4.1. Short application description

Data storage technologies include ‘solid-state’ storage such as DRAM and Flash, and storage technologies with a mechanical component, including hard disk drives. Data storage applications include:

- Computers (which would commonly contain both RAM and a hard disk drive)
- Mobile Devices (in which the memory media is more likely to be a memory card, commonly Secure Digital (SD) format)
- Portable media players (the first generation iPods used a hard disk drive produced by Toshiba, but later versions has switched to flash memory storage.)

There are a number of nanotechnology-based approaches to the development of data storage which are described in the technology sector report and which are briefly summarised here:

- Magnetoresistive Random Access Memory (MRAM), in which each memory cell consists of two ferroelectric plates, sandwiching an insulating layer
- Ferroelectric RAM (FeRAM), similar to DRAM but for the fact that a ferroelectric layer is substituted for the dielectric layer.
- Resistive RAM (RRAM), in which a conduction path is created in a dielectric material
- NRAM (Nanotube RAM), a trademark of Nantero, using the positing of carbon nanotubes to determine memory states.

4.4.2. Functional requirements

Functional requirements of data storage include the following:

Capacity

Capacity is a measure of the amount of data (in MB, megabytes) that can be stored on a given memory type. To give an example of a product currently on the market, Seagate currently sells hard disk drives with a memory capacity of 1 500 000 MB, or 1.5 terabytes (TB). SanDisk sells

Flash memory with capacities of up to 16 GB for imaging and mobile applications, and sells solid state drives with up to 240 GB as hard disk drive replacements²⁸.

Memory Density

Memory density is a function of capacity and size, and is typically driven by the size of individual memory cells (and the amount of data that each cell can store). Multi-level cells enable the storage of multiple data bits per cell – Fujitsu reported Flash memory with 4 bits per cell in 2007²⁹.

Lifetime

The target lifetime of a data storage application is measured in read/write cycles (lifetimes expressed in years are sometimes used, but these are an average of the expected read/write cycles per day). Flash memory will degrade over time. Memory manufacturer Kingston Technology claims that its Flash Multi-Level Cells last for 10,000 read/write cycles, and its Single Level Cells for 100,000 cycles³⁰. Alternative nanotechnology-based approaches, such as MRAM, should demonstrate improved endurance.

Read/Write Speed

As an electromechanical device, hard disk drives have a time lag between receiving an instruction to access memory and actually being able to read or write it (as the disk has to be rotated to the correct location, and the read/write head has to be moved). These delay times are usually measured in milliseconds. Solid state memory has much quicker access times.

Cost

As with many of the applications described in this report, cost is a function of the manufacturing efficiency and defect rate. The production of Flash memory is now a highly optimised process, which has demonstrated dramatic scaling improvements.

²⁸ <http://www.sandisk.com>

²⁹ <http://www.fujitsu.com/downloads/EDG/binary/pdf/find/25-1e/3.pdf>

³⁰ http://www.kingston.com/products/pdf_files/FlashMemGuide.pdf

Volatility

Data storage is non-volatile if it maintains the contents of memory without power. The primary volatile memories currently in use are SRAM and DRAM. A ‘universal memory’ would combine the speed of SRAM and DRAM with non-volatility.

4.4.3. Boundary conditions

Whilst CMOS compatibility is not per se a boundary condition for all data storage applications, it is an important factor in ensuring ease of integration and cost effectiveness of manufacturing.

4.4.4. Product examples

Everspin MRAM

Freescale Semiconductor released a 4Mb MRAM product in 2006, which is believed to be the first commercially available MRAM product, and which won a number of awards at that time. At the beginning of 2008, an MRAM module was included in a magnetometer subsystem on a Japanese satellite. The selection of MRAM seems to have been influenced by its greater endurance and extended temperature operation³¹. Subsequently, Freescale’s MRAM business was spun out to form a new company, Everspin³².

4.4.5. Economic Information and Analysis

A 2005 study by NanoMarkets projected that nanotechnology-enabled storage devices would be a \$65,7bn market by 2012³³; accounting for 40% of the total memory market.

Relatively few nanotechnology enabled storage technologies are known to be available at this time.

³¹ <http://media.freescale.com/phoenix.zhtml?c=196520&p=irol-newsArticle&ID=1111857&highlight=>

³² http://www.eetasia.com/ART_8800528389_499486_NT_49445c1e.HTM

³³ NanoTechWire, <http://nanotechwire.com/news.asp?nid=1059&ntid=123&pg=11>

4.4.6. Selected Key Companies Profiles

Ramtron

Ramtron (<http://www.ramtron.com/>) sells FeRAM products and integrated solutions for a number of applications areas, including automotive, computing, and metering.

Nantero

Nantero (<http://www.nantero.com>) develops NRAM, a registered trademark of the company. NRAM was developed by Thomas Rueckes, who is currently the CTO of the company. Nantero has developed a number of prototype devices, including one with an array of 10 million nanotube junctions. The company has priorities compatibility with existing semiconductor manufacturing processes.

Crocus Technology

Crocus (<http://www.crocus-technology.com>) claims to have addresses a number of the problems associated with MRAM, including thermal sensitivity. The company is currently moving from a development to early commercialisation stage. Crocus has locations in Silicon Valley and Grenoble.

5. Expert Engagement

Experts who attended the ObservatoryNano symposium in March 2009 included:

Dr. Dirk Holtmannspötter (Zukuenftige Technologien Consulting),

Axel Schindler (Display Technology, University of Stuttgart),

Dr. Volkhard Beyer (Fraunhofer Center Nanoelektronische Technologien),

Dr. Inger Vikholm-Lundin (VTT),

Dr. Daping Chu (CAPE, Cambridge)

Input was also derived from a number of contributions to Nanotech Northern Europe 2008, including:

Vladimir Ermolov, Nokia

Stuart Parkin, IBM

Stan Williams, HP

Lars Erik Wernersson, Lund University

Christian Joachim, CEMES

Nikolai Ledentsov, TU Berlin

Jong Min Kim, Samsung

Andre Geim, Manchester

Yuji Awano, Fujitsu